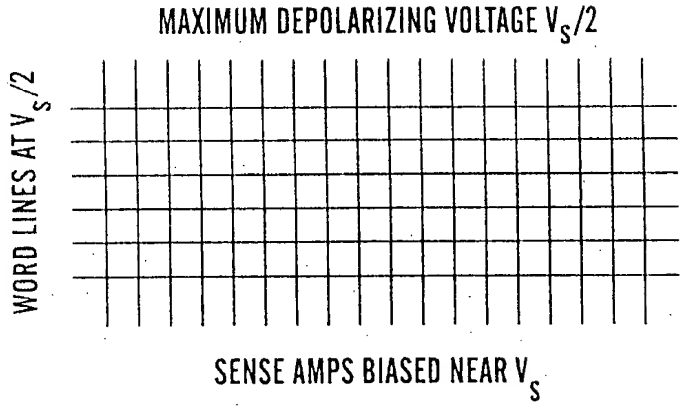
Approved
4/22/03

- t_0: WORD LINE LATCHED, ACTIVE PULLDOWN TO 0
- t_1: BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2: BIT LINE DECISION - DATA LATCHED
- t_3: WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_4: WRITE DATA LATCHED ON BIT LINES
- t_5: WORD LINE PULLED TO V_s - SET/RESET ~~CAPS~~ CELL
- t_6: WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_7: BIT LINES ACTIVELY RETURNED TO V_s CLAMP
- t_8: READ/WRITE CYCLE COMPLETE



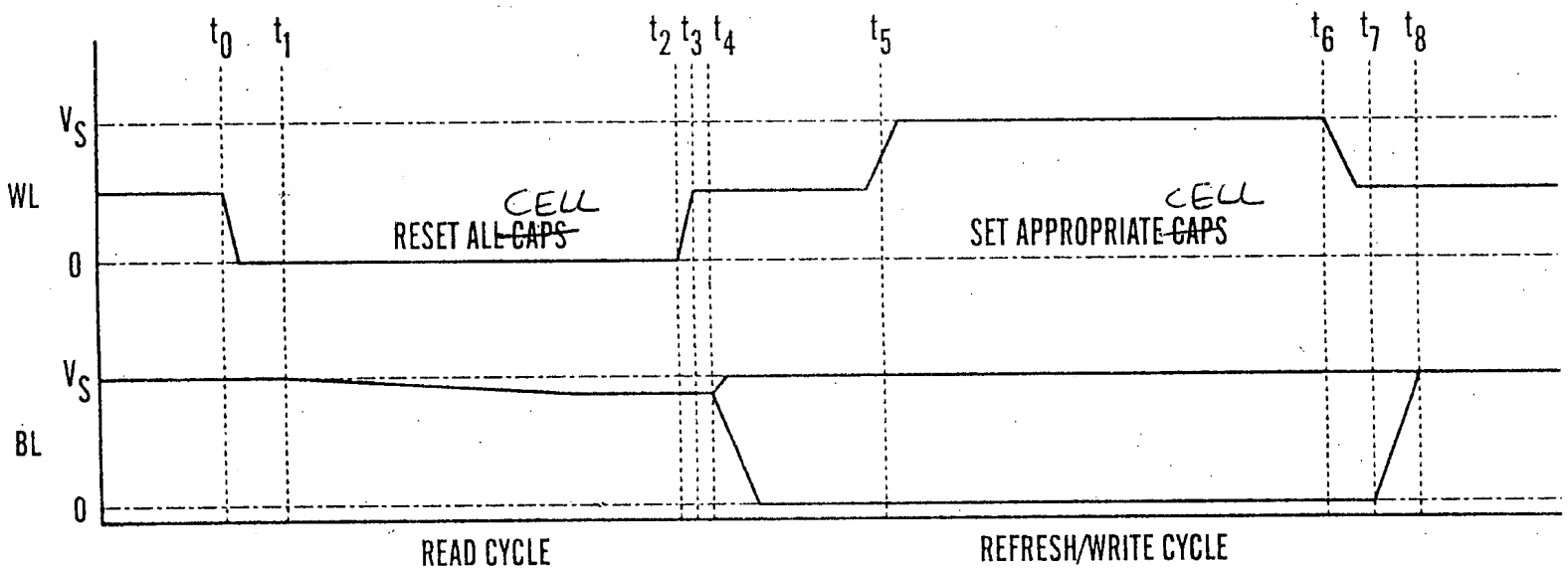
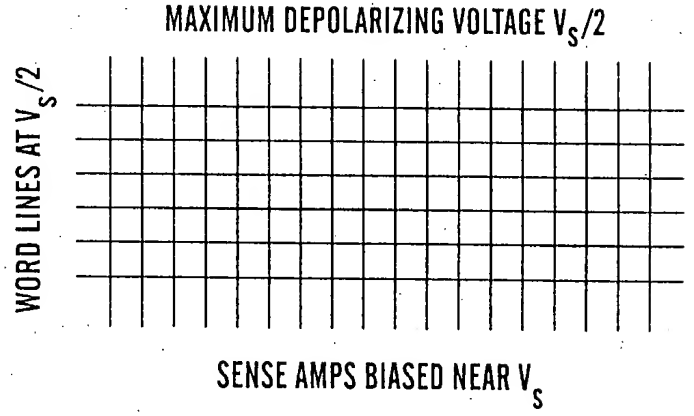


Fig.4

- t_0: WORD LINE LATCHED, ACTIVE PULL UP TO V_s
- t_1: BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2: BIT LINE DECISION - DATA LATCHED
- t_3: WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_4: WRITE DATA LATCHED ON BIT LINES
- t_5: WORD LINE PULLED TO 0 - SET/RESET ~~CAPS~~ CELL
- t_6: WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_7: BIT LINES ACTIVELY RETURNED TO 0 CLAMP
- t_8: READ/WRITE CYCLE COMPLETE



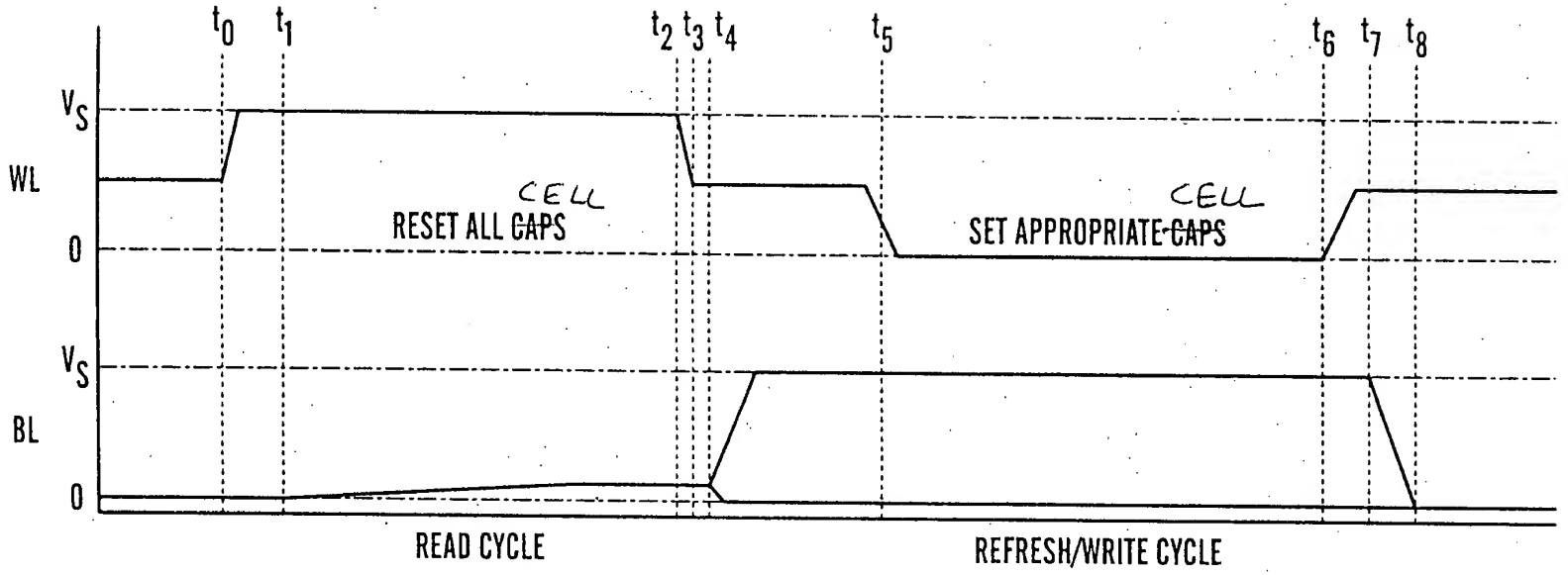


Fig.5